COURSE STRUCTURE
AND
DETAILED SYLLABUS
(MR12Regulations)

for

M.Tech (Digital Systems & Computer Electronics)

(Applicable for the batches admitted from 2012-13)

MALLA REDDY ENGINEERING COLLEGE

(Autonomous)

Maisammaguda, Dhulapally (PO) Via (Hakimpet), Hyderabad- 500 014.

www.mrec.ac.in **E-mail: mrec.2002@gmail.com**

MALLA REDDY ENGINEERING COLLEGE
(Autonomous)
Maisammaguda, Dhulapally (Post via Hakimpet), Secunderabad – 500 014.

August/September 2012

Academic Regulations 2012 for M.Tech. (Regular)
(*Effective for the students admitted into first year from the academic year 2012-2013*)

The M.Tech Degree of Malla Reddy Engineering College, Hyderabad shall be conferred on candidates by the Jawaharlal Nehru Technological University Hyderabad (JNTUH), Hyderabad who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 ELIGIBILITY FOR ADMISSIONS:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by the university/college from time to time.

Admissions shall be made on the basis of merit rank obtained by the qualifying candidate at an Entrance Test conducted by the university/college or on the basis of any other order of merit approved by the university/college (say **PGECET / GATE)** subject to reservations prescribed by the university/college from time to time.

Candidates seeking admission to programmes on a part time basis should be working in or around the place where the programme is being run after passing qualifying examination.

2.0 AWARD OF M. TECH. DEGREE:

2.1 A student shall be declared eligible for the award of the M.Tech degree, if he pursues a course of study and completes it successfully for not less than two academic years and not more than four academic years.

2.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his admission, shall forfeit his seat in M.Tech course.

2.3 The minimum instruction for each semester 90 clear instruction days.

3.0 A. COURSE OF STUDY:

A candidate after securing admission must pursue the prescribed course of study for the following duration.

M.Tech - Four Semesters

Each Semester shall be of 22 Weeks of duration including examinations.

A candidate admitted to a programme should complete it within a period equal to twice the prescribed duration of the programme from the date of admission.

The following specializations are offered at present for the M.Tech course of study..

1. Control Engineering
2. Computer Science and Engineering
3. Computer Science
4. Control Systems
5. Digital Systems & Computer Electronics
6. Structural Engineering
7. Thermal Engineering
8. Transportation Engineering
9. VLSI System Design

and any other course as approved by the authorities of the university/college from time to time.

Each subject is assigned certain number of credits depending upon the number of contact hours as follows.

Theory subjects	***4 Periods / Week***	***3 Credits***
Practical/ Drawing	***4 Periods / Week***	***2 Credits***
Seminar	***_***	***2 Credits***

Comprehensive Viva – Voce/ Independent Study 2 Credits
Project Work 40 Credits
(Each period will be of 50 minutes duration)

3.0 B. Departments offering M. Tech Programs with Specializations mentioned below:

Civil Engineering Department	1. Structural Engineering 2. Transport Engineering
Computer Science & Engineering Department	1. Computer Science & Engineering 2. Computer Science
Electrical Electronics Engineering Department	1. Control Systems 2. Control Engineering
Electronics & Communication Engineering Department	1. Digital Systems & Computer Electronics 2. VLSI System Design
Mechanical Engineering Department	1. Thermal Engineering

4.0 ATTENDANCE:
The programs are offered on a unit basis with each subject being considered unit.
4.1 A candidate shall be deemed to have eligibility to write end semester examinations in a subject if he has put in at least 65% of attendance in that subject.

4.2 ***Shortage of attendance up to 10% in any subject (i.e. 65% and above and below 75%) may be condoned by the College Academic Committee on genuine and valid reasons on representation by the candidate with supporting evidence.***
4.3 A candidate shall get minimum required attendance at least in three (3) theory subjects in the present semester to get promoted to the next semester. In order to qualify for the award of the M.Tech. Degree, the candidate shall complete all the academic requirements of the subjects, as per the course structure.

4.4 ***Shortage of attendance below 65% shall in no case be condoned.***

4.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

5.0 EVALUATION:
The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory and 100 marks for practical, on the basis of Internal Evaluation and End Semester Examination.

5.1 For the theory subjects 60 marks shall be awarded based on the performance in the End Semester Examination, 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be made based on the better of the marks secured in the two Mid Term-Examinations conducted one in the middle of the Semester and the other immediately after the completion of instruction each for a total of 30 marks. Each mid term examination shall be conducted for a duration of 120 minutes with 4 questions to be answered out of 6 questions. In addition, there shall be two assignments evaluated for 10 marks each and average of the two taken as the final assignment mark. The sum of the best of the two mid examinations and the assignment marks obtained shall be the final marks for internal evaluation.

5.2 For practical subjects, 60 marks shall be awarded based on the performance in the End Semester Examinations, 40 marks shall be awarded based on the day-to-day performance as internal Marks.
And 25 marks to be awarded by conducting an internal laboratory test. The End Examination shall be conducted by the teacher concerned and another faculty member of the same Department, as suggested by the Head of Department.

5.3 There shall be two seminar presentations during I year I semester and II Semesters. For seminar, a student under the supervision of a faculty member, shall collect the literature on a topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the

Department, supervisor and two other senior faculty members of the department. For each Seminar there will be only internal evaluation of 50 marks. A candidate has to secure a minimum of 50% to be declared successful. *There shall be no external examination for Seminar*

5.4 Every candidate shall be required to execute his P.G. Project and submit his Dissertation, after taking up a topic approved by the Project Review Committee (PRC). The PRC shall be constituted by the Head of the Department, and shall consist of the Head of the Department, the Project supervisor, and a Senior faculty member of the Department. The PG project shall start immediately after completion of the I Year II Semester, and shall be of one year duration. The student has to decide his topic for his M.Tech Project Work within the first 6 weeks of the summer vacation at the end of the II semester and should submit his PG Project Work Proposal to the PRC, on whose approval he can register for the PG project. The PRC will monitor the progress of the project work through Two-Seminar presentations – one during II Year I Semester, and one before the submission of the PG Project/ Dissertation. The student shall submit a project Report at the end of that semester by the PRC as SATISFACTORY or UNSATISFACTORY. In the case of Unsatisfactory declaration, the student shall resubmit the Project report after carrying out the necessary modifications / additions in the Project work, within the specified time as suggested by the PRC. The student can submit the Dissertation, only after completion of 40 weeks from the Date of Registration, after obtaining the approval from PRC. Extension of time, within the total permissible limit for the completion of the Degree, may be considered by the PRC, on sufficient valid/ genuine grounds.

5.5 There shall be a Seminar presentation in the II year I Semester, for the award of 50 marks. The seminar shall be on the topic chosen for PG Project/ Dissertation Work and the assessment will be done by the same PRC as constituted above. There shall be no external marks for the Seminar.

There shall be a Comprehensive Viva-Voce in II year II Semester. The Comprehensive Viva-Voce will be conducted by a Committee consisting of Head of the Department and two Senior Faculty members in that area of specialisation. The Comprehensive Viva-Voce is aimed to assess the students' understanding in various subjects he/she studies during the M.Tech course of study. The Comprehensive Viva-Voce is valued for 100 marks by the Committee. There are no internal marks for the Comprehensive viva-Voce

5.6 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

5.7 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.4) he has to reappear for the End Examination in that subject. A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and he has failed in the end examination. In such case candidate must re-register for the subject(s) and secure required minimum attendance. Attendance in the re-registered subject(s) has to be calculated separately to become eligible to write the end examination in the re-registered subject(s). The attendance of re-registered subject(s) shall be calculated separately to decide upon the eligibility for writing the end examination in those subject(s). In the event of taking another chance, the internal marks and end examination marks obtained in the previous attempt are nullified.

5.8 In case the candidate secures less than the required attendance in any subject(s), he shall not be permitted to appear for the End Examination in that subject(s). He shall re-register the subject when next offered.

5.9 Laboratory examination for M.Tech courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be other Laboratory Teacher or any other member from inside/outside of the college.

6.0 EVALUATION OF PROJECT/ DISSERTATION WORK:

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Project Review Committee.

6.1 A Project Review Committee (PRC) shall be constituted with Principal as chair person Heads of all the Departments which are offering the M.Tech programs and two other senior faculty members.

6.2 Registration of Project Work: A candidate is permitted to register for the project work after satisfying the attendance requirement of all the subjects (theory and practical subjects).

6.3 After satisfying 6.2, a candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work to the Departmental Committee for its approval. Only after obtaining the approval of Departmental Committee the student can initiate the Project work. ***Departmental Committee Consists of Head of the Department as Chairman, along with two Senior Professors and few subject experts too.***

6.4 If a candidate wishes to change his supervisor or topic of the project he can do so with approval of Departmental Committee. However, the Departmental Committee shall examine whether the change of topic/supervisor leads to a major change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.5 Candidate shall submit status report (in a bound-form) in two stages at least with a gap of 3 months between them.

6.6 The work on the project shall be initiated in the beginning of the second year and the duration of the project is for two semesters. A candidate is permitted to submit Project Thesis only after successful completion of theory and practical course with the approval of PRC not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Principal (through Head of the Department) and shall make an oral presentation/demonstration before the PRC.

6.7 Three copies of the Project Thesis certified by the supervisor shall be submitted to the College / School/ Institute.

6.8 The thesis shall be adjudicated by one examiner selected by the College. For this, Head of the Department shall submit a panel of 5 examiners to the Principal of the College, who are eminent in that field with the help of the concerned guide and Head of the department.

6.9 If the report of the examiner is not favorable, the candidate shall revise and resubmit the Thesis, in the time frame as described by PRC. If the report of the examiner is unfavorable again, the thesis shall be summarily rejected.

6.10 If the report of the examiner is favorable, viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the Thesis. The Board shall jointly report candidates work as:

A. Excellent
B. Good
C. Satisfactory
D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination.

If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination after three months. If he fails to get a satisfactory report at the second viva-voce examination, he will not be eligible for the award of the degree unless he is asked to revise and resubmit by the Board.

7.0 AWARD OF DEGREE AND CLASS:

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following four classes:

Class Awarded	% of marks to be secured	*Program Credits*
First Class with Distinction	70% and above	***From the Aggregate secured for all the 88 credits***
First Class	Below 70% but not less than 60%	
Second Class	Below 60% but not less than 50%	
Pass Class	Below 50% but not less than 40%	

(The marks in internal evaluation and end examination shall be shown separately in the marks memorandum)

8.0 WITH-HOLDING OF RESULTS:

If the candidate has not paid any dues to the university or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed into the next higher semester. The issue of the degree is liable to be withheld in such cases.

9.0 TRANSITORY REGULATIONS:

Candidate who have discontinued or have been detained for want of attendance or who have failed after having undergone the course are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to rule 5.5 and 2.0 of these regulations.

10.0 GENERAL:

10.1 The academic regulations should be read as a whole for purpose of any interpretation.

10.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Principal is final.

10.3 The College may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the College.

10.4 Wherever the word he, him or his occur, it will also include she, her and hers.

10.5 Wherever the word 'Subject' occurs in the above regulations, it implies the 'Theory Subject' and 'Practical Subject' or 'Lab'.

10.5 Transfers not allowed among group colleges.

MALLA REDDY ENGINEERING COLLEGE (*AUTONOMOUS*)
Department of Electronics & Communication Engineering
M.TECH (DSCE-FULL TIME) 2012-13 SCHEME

I SEMESTER

Code	Subject	L	T	P	credits	Int. Evaluation	End exam
MR124101	VLSI Technology & Design	3	1	0	3	40	60
MR124102	Digital System Design	3	1	0	3	40	60
MR124103	Coding Theory & Techniques	3	1	0	3	40	60
MR124104	Advanced Data Communications	3	1	0	3	40	60
MR124105 MR124106 MR124107	Elective 1 Advanced Digital Signal Processing Image & Video Processing Biomedical Instrumentation	3	1	0	3	40	60
MR124108 MR124109 MR124110	Elective 2 FPGA Architectures Applications Digital Control systems Internetworking	3	1	0	3	40	60
MR124111	Simulation Lab(VHDL/VERILOG)	0	0	3	2	40	60
MR124112	Seminar	-	-	3	2	50	
	Total	18	6	6	22	330	420

II SEMESTER

Code	Subject	L	T	P	credits	Int. Evaluation	End exam
MR124113	Advanced Computer Architecture	3	1	0	3	40	60
MR124114	Low Power VLSI Design	3	1	0	3	40	60
MR124115	Design of Fault Tolerant Systems	3	1	0	3	40	60
MR124116	Embedded system Design &RTOS	3	1	0	3	40	60
MR124117 MR124118 MR124119	Elective 3 System on Chip Architecture Network Security &Cryptography Robotics	3	1	0	3	40	60
MR124120 MR124121 MR124122	Elective 4 CMOS Analog &Mixed Signal Design Digital Signal Processor Architectures Artificial Intelligence	3	1	0	3	40	60
MR124123	Embedded System Design lab	0	0	3	2	40	60
MR124124	Seminar	-	-	3	2	50	
	Total	18	6	6	22	330	420

III SEMETER

Code	Subject	L	T	P	credits	End exam
MR124125	Comprehensive Viva	-	-	-	2	100
MR124126	Project Seminar	-	-	6	2	-
MR124127	Project work	-	-	-		-
	Total	-	-	6	4	100

IV SEMESTER

Code	Subject	L	T	P	credits	End Exam
MR124128	Project work & Seminar	-	-	-	40	Grade
	Grade (A/B/C/D)					A. Excellent B. Good C. Satisfactory D. Unsatisfactory

2012-13 **MR124101**

MALLA REDDY ENGINEERING COLLEGE
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M. TECH-DSCE-I SEMESTER

L	T/P/D	c
3	1/-/-	3

VLSI TECHNOLOGY AND DESIGN

UNIT – 1

Review of Microelectronics and Introduction to MOS Technologies: MOS, CMOS, BiCMOS Technology, Trends and Projections

Basic Electrical Properties of MOS, CMOS & BiCMOS Circuits I_{ds} – V_{ds} relationships. Threshold Voltage V , G, G and U Pass Transistor, MOS, CMOS & BiCMOS Interters, Zpu/Zpd, MOS Transistor circuit model, Latch-up in CMOS circuits.

UNIT – II

LAYOUT DESIGN AND TOOLS: Transistor structures, wires and Vias, Scalable Design rules, Layout Design tools.

LOGIC GATES & LAYOUTS Static Complementary Gates, Switch Logic, Alternative Gate circuits, Low power gates, Resistive and inductive interconnect delays.

UNIT – III

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network delay, Interconnect design, Power optimization, Switch logic networks, Gate and Network testing

UNIT – IV

SEQUENTIAL SYSTEMS: Memory cells and Array, Clocking disciplines, Design, Power optimization, Design validation and testing.

UNIT – V

FLOORING PLANNING & ARCHITECTURE DESIGN: Floor planning methods, off-chip connections, High-level synthesis, Architecture for low power, SOCs and Embedded CPUs, Architecture testing.

TEXT BOOKS:

1. Essentials of VLSI Circuits and Systems, K. Eshraghian Eshraghian, D.A.Pucknessl, 2005, PHI.
2. Modern VLSI Design – Wayne Wolf, 3rd ed. 1997, Pearson Education.

REFERENCES:

1. Principals of CMOS VLSI Design – N H E Weste, K.Eshraghian, 2nd ed. Adisson Wesley

2012-13 **MR124102**

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L	**T/P/D**	**C**
3	**1/-/-**	**3**

M. TECH-DSCE-I SEMESTER

DIGITAL SYSTEM DESIGN

UNIT-I

DESIGNING WITH PROGRAMMABLE LOGIC DEVICES

Designing with Read only memories – Programmable Logic Arrays – Programmable Array logic – Sequential Programmable Logic Devices – Design with FPGA's – Using a one-hot stage assignment.

State transition table – State assignment for FPGA's Proglem of initial state assignment for One – Hot encoding – State Machine Charts – Derivation of SM Charts – Realization of SM Charts – Design Examples – Serial adder with Accumulator – Binary Multiplier – Signed Binary number multiplier (2's Complement multiplier) – Binary Divider – Control logic for Sequence detector – Realization with Multiplexer – PLA – PAL

UNIT – II

FAULT MODELING & TEST PATTERN GENERATION

Logic Fault model – Fault detection & Redundancy – Fault equivalence and fault location – Fault dominance – Single stuck at fault model – Multiple stuck at fault models – Bridging fault model.

Fault diagnosis of combinational circuits by conventional methods – Path sensitization techniques, Boolean Difference method – Kohavi algorithm – Test algorithms – D algorithm, PODEM, Random testing. Transition count testing, Signature analysis and test bridging faults.

UNIT – III

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS

Circuit Test Approach, Transition Check Approach – State identification and fault detection experiment. Machine nidentification, Design of fault detection experiment.

UNIT – IV

PLA MINIMIXATION AND TESTING

PLA minimization – PLA folding, Fault model in PLA, Test generation and Testable PLA Design.

UNIT – V

MINIMIZATION AND TRANSFORMATION OF SEQUENTIAL MACHINES

The finite state Model – Capablities and limitations of FSM – State equivalence and machine minimization – Simplification of incompletely specified machines.

Fundamental mode model – Flow table – State reduction – Minimal closed covers – Races. Cycles and Hazards.

Text Books

Fundamentals of Logic Design – Charles H Roth, 5th ed. Cengage Learning

Digital Systems Testing and Testable Design – Miron Abramovici, Melvin A, Breuer and Arthur D. Friedman – John Wiley & Sons Inc.

Logic Design Theory – N.N.Biswas, PHI

Reference Books:

Switching and Finite Automata Theory – Z. Kohavi, 2nd ed. 2001, TMH

Digital Design – Morris Mano, M.D.Ciletti, 4th Edition, PHI

Digital Circuits and Logic Design – Samuel C. Lee, PHI

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M. TECH-DSCE-I SEMESTER

L	T/P/D	C
3	1/-/-	3

CODING THEORY AND TECHNIQUES

UNIT – I: Source coding: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, coding for discrete less sources, Source coding theorem, fixed length and variable length coding, properties of prefix codes,Shannon-Fano coding, Huffman code, Huffman code applied for pair of symbols, efficiency calculations, Lempel-Ziv codes.

UNIT – II: Linear Block codes: Introduction to Linear block codes, Generator Matrix, Systematic Linear Block codes, Encoder Implementation of Linear Block Codes, Parity Check Matrix, Syndrome testing, Error Detecting and correcting capability of Linear Block codes. Hamming Codes, Probability of an undetected error for linear codes over a Binary Symmetric Channel, Weight Enumerators and Mac-Williams identities, Perfect codes, Application of Block codes for error control in data storage Systems.

UNIT – III: Cyclic Codes: Algebraic structure of cyclic codes, Binary Cyclic code properties, Encoding in systematic and non-systematic form, Encoder using (n-k) bit shift register, Syndrome Computation and Error detection, Decoding of Cyclic Codes.

UNIT –IV: Convolutional Codes: encoding of Convolutional codes, Structural properties of Convolutional codes, state diagram, Tree diagram, Trellis Diagram, maximum, Likelihood decoding of Convolutional codes.Viterbi Algorithm, Fano, Stack Sequential decoding algorithms, Application of Viterbi and sequential decoding.

UNIT – V: BCH Codes: Groups, fields, binary Fields arithmetic, construction of Falois fields GF (2m), Basic properties of Falois Fields, Computation using Falois Field GF (2m) arithmetic, Description of BCH codes, Decoding procedure for BCH codes.

TEXT BOOKS:

1. Error Control Coding – Fundamentals and Applications by SHU LIN and Daniel J. Costello, Jr. Prentice
Hall Inc.
2. Digital Communications – Fundamental and Application by Bernard sklar, Pearson Education Asia.
3. Error Control Coding Theory by Man Young Rhee, Mc. Graw Hill Publ.

REFERENCE BOOKS:

1. Digital Communications – John G. Proakis, Mc. Graw Hill Publication.
2. Digital and Analog Communication Systems – K. Sam Shanmugam
3. Digital Communications by Symon Haykin.

2012-13 **MR124104**

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M. TECH-DSCE-I SEMESTER

L	T/P/D	C
3	1/-/-	3

ADVANCED DATA COMMUNICATIONS

UNIT-I

Digital Modulation: Introduction, Information Capacity Bits, Bit Rate, Baud, and M.ARY Coding, ADK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, DPSK – Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT-II

Basic concepts of Data Communications, Interfaces and Modems: Data Communication Components , Networks, Distributed Processing, Network Criteria – Applications, Protocols and Standards, Standards Organizations – Regulatory Agencies. Line configuration – Point-to-Point-Multipoint, Topology – Mesh – Star – Tree – Bus – Ring – Hybrid Topologies. Transmission Modes-Simplex-Half duplex- Full Duplex, Categories of Net works – LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE – DCE Interface-Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems-Transmission Rates.

UNIT-III

Error Detection and Correction: Types of Errors – Single Bit Error, CRC (Cyclic Redundancy Check) performance, Checksum, Error Correction Single Bit Error Correction, Hamming Code.

Data Link Control: Stop and Wait, Sliding Window Protocols.

Data Link Protocols: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol-Binary Synchronous Communication (BSC) – BSC Frames – Data Transparency, Bit Oriented Protocols – HDLC Link Access Protocols.

UNIT-IV

Switching: Circuit Switching – Space Division Switches – Time Division Switches – TDM Bus-Space and Time Division Switching Combinations – Public Switched Telephone Network, Packet Switching-Datagram Approach- Virtual Circuit Approach- Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

Multiplexing: Time Division Multiplexing (TDM) Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

UNIT-V

Multiple Access: Random Access Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/DA) Controlled Access- Reservation- Polling- Token Passing, Channelization-Frequency- Division Multiple Access (FDMA), Time – Division Multiple Access (TDMA), - Code – Division Multiple Access (CDMA).

Text Books:

Data Communication and Computer Networking – B.A.Forouzan, 3rd ed.2008, TMH

Advanced Electronic Communication Systems – W.Tomasi, 5ed. 2008, PEI.

Reference:

Data Communications and Computer Nerworks – Prakash C.Gupta, 2006, PHI

Data and Computer Communications – William Stallings, 8th ed.2007, PHI

Data Communication and Tele Processing Systems-T.Housely, 2nd Edition,208 BSP.

Data Communications and Computer Networks – Brijendra Singh, 2nd ed.2005, PHI

2012-13 **MR124105**

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M. TECH-DSCE-I SEMESTER

ADVANCED DIGITAL SIGNAL PROCESSING

(Elective I)

UNIT – I:

Review of DFT, FFT, IIR Filters, FIR Filters

MultiRate Signal Processing: Introduction, Decimation by a factor D. Interpolation by a factor I. sampling rate conversion by a rational factor I/D. Multistage Implementation of Sampling Rate Conversion, Filter design & Implementation for sampling rate conversion, Applications of Multirate Signal Processing.

UNIT – II

Non-Parametric methods of Power Spectral Estimation: Estimation of spectra from finite duration observation of signals, Non-parametric Methods: Bartlett, Welch & Blackman & Tukey methods, Comparison of all Nonm-Parametric methods.

UNIT – III

Parametric Methods of Power Spectrum Estimation: Autocorrelation & its Properties, Relation between auto correlation & model parameters, AR Models – Yule-Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

UNIT – IV

Implementation of Digital Filters

Introduction to filter structures (IIR & FIR), Frequency sampling structures of FIR, Lattice structures, Forward prediction error, Backward prediction error, Reflection coefficients for lattice realization, implementation of lattice structures for IIR filters, Advantages of lattice structures.

UNIT – V

Finite Word Length Effects: Analysis of finite word length effects in Fixed-Point DSP Systems – Fixed, Floating Point Arithmetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

TEXTBOOKS:

Digital Signal Processing, Principles, Algorithms & Applications – J.G.Proakis & D.G. Manolokis, 4th ed. PHI

Discrete Time signal processing – Alan V Oppenheim & Ronald W.Schaffer, PHI

DSP – A Practical Approach – Emmanuel C.Ifeacher, Barrie, W.Jervis, 2ed. Pearson Education

REFERENCES:

Modern nspectral Estimation : Theory & Application – S.M.Kay, 1988 PHI.

Multirate Systems and Filter Banks – P.P.Vaidyanathan – Pearson Education

Digital Signal Processing – S.Salivahanan, A.Vallavaraj, C.Gnanapriya, 2000, TMH

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M. TECH-DSCE-I SEMESTER

IMAGE & VIDEO PROCESSING

(Elective I)

UNIT-I: Fundamentals of Image Processing and Image Transforms:

Basic steps of Image Processing System Sampling and Quantization of an image – Basic relationship between pixels

Image Transforms: 2 D-Discrete Fourier Transform, Discrete Cosine Transform (DCT), Wavelet Transforms: Continuous Wavelet Transform, Discrete Wavelet Transforms.

UNIT II Image Processing Techniques

Image Enhancement

Spatial domain methods: Histogram Processing, Fundamentals of Spatial filtering, Smoothing spatial filters, Sharpening spatial filters.

Frequency domain methods: Basics of filtering in frequency domain, image smoothing, image sharpening, Selective filtering.

Image Segmentation Segmentation concepts, Point, Line and Edge Detection, Thresholding, Region Based segmentation.

UNIT III: Image Compression

Image compression fundamentals – Coding Redundancy, Spatial and Temporal redundancy, Compression models: Lossy & Lossless, Huffman coding, Arithmetic coding, LZW coding, Run length coding, Bit plane coding, Transform coding, Predictive coding, Wavelet coding, JPEG Standards.

UNIT – IV: Basic steps of Video Processing

Analog Video, Digital Video, Time-Varying Image Formation models: Three-Dimensional Motion Models, Geometric Image Formation, Photometric Image Formation, Sampling of Video signals, Filtering operations.

UNIT – V: 2-D Motion Estimation

Optical flow, General Methodologies, Pixel Based Motion Estimation, Block- Matching Algorithm, Mesh based Motion Estimation, Global Motion Estimation, Region based Motion Estimation, Multi resolution motion estimation, Waveform based coding, Block based transform coding, Predictive coding, Application of motion estimation in Video coding.

TEXT BOOKS:

1. Digital Image Processing- Gonzaleze and Woods, 3rd ed. – Pearson.
2. Video processing and communication – Yao Wang, Joem Ostermann and Ya-quin Zhang, 1st Ed. PH Int.

REFERENCE BOOKS:

1. Digital Video Processing – M.Tekalp, Prentice Hall International

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M. TECH-DSCE-I SEMESTER

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BIO-MEDICAL INSTRUMENTATION

(ELECTIVE – I)

UNIT I

Components of Medical Instrumentation System. Bioamplifier. Static and dynamic characteristics of medical instruments. Biosignals and characteristics. Problems encountered with measurements from human beings.

UNIT II

Organisation of cell. Derivation of Nernst equation for membrane Resting Potential Generation and Propagation of Action Potential, Conduction through nerve to neuro-muscular junction.

Bio Electrodes – Biopotential Electrodes-External electrodes, Internal Electrodes. Biochemical Electrodes.

UNIT III

Mechanical function, Electrical Conduction system of the heart. Cardiac cycle. Relation between electrical and mechanical activities of the heart.

Cardiac Instrumentation Blood pressure and Blood flow measurement. Specification of ECG machine. Einthoven triangle, Standard 12-lead configurations, Interpretation of ECG waveform with respect to electro mechanical activity of the heart.

UNIT IV

Therapeutic equipment. Pacemaker, Defibrillator, Shortwave diathermy. Hemodialysis machine.

Respiratory Instrumentation Mechanism of respiration, Spirometry, Pnemuotachograph Ventilators.

UNIT V

Neuro-Muscular Instrumentation Specification of EEG and EMG machines. Electrode placement for EEG and EMG recording. Intrepretation of EEG and EMG.

TEXT BOOKS :

1. Biomedical Instrumentation and Measurements – Leslie Cromwell and F.J. Weibell,E.A.Pfeiffer,2nd ed 1980, PHI.

2. Medical Instrumentation, Application and Design – John G. Webster, 3rd Ed., 1998, John Wiley.

REFERENCES :

1. Principles of Applied Biomedical Instrumentation – L.A. Geoddes and L.E. Baker, 1975, John Wiley.

2. Hand-book of Biomedical Instrumentation – R.S. Khandpur, 2nd ed., 2003, TMH.

3. Biomedical Telemetry – Mackay, Stuart R1968, John Wiley.

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M. TECH-DSCE-I SEMESTER

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FPGA ARCHITECTURE AND APPLICATIONS

(Elective II)

UNIT – I:

Programmable logic: ROM, PLA, PAL PLD, PGA – Features, programming and applications using complex programmable logic devices Altera senses – Max 5000/7000 series and Altera FLEX logic 10000 senses CPLD, AMD'S – CPLD (Mach 1 to 5) Cypres FLASH 370 Device technology, Lattice PLST's architectures – 3000 series – Speed performance and in system programmability.

UNIT – II

FPGA'S Field Programmable gate arrays – Logic blocks, routing architecture, design flow technology mapping jfor FPGAs Cse studies Xitir x XC4000 & ALTERA's FLEX 8000/10000 FPGAs : AT & T ORCA's (Optimized Reconfigurable Cell Array) ACTEL's ACT-1,2,3 and their speed performance.

UNIT – III

Alternative realization for state machine charts using microprogramming linked state machine one – hot state machine, petrinets for state machines-basic concepts, properties, and extended petrinets for parallel controllers.

UNIT – IV

Digital front end digital design tools for FPGAs & ASICs: Using mentor graphics EDA tool (FPGA Advantage") – Design flow using FPGAs

UNIT – V

Introduction To TMS 320c54xx And TMS 320c60xx And Its Architectures, Introduction To Dsp Based FPGA

SUGGESTED BOOKS:

1. Field Programmable Gate Array Technology – S>Trimberger, Edr. 1994, Kluwer Academic Publications
2. Field Programmable Gate Arrays John V.Oldfield Richard C.Dore Wiley Publications

Reference Books:

1. Digital Design Using Field Programmable Gate Array, P.K.Chan & S.Mourad, 1994, Prentice Hall.
2. Digital System Design using Programmable Logic Devices– Parag.K.Lala, 2003, BSP
3. Field programmable gate array, S.Brown, R.J.Francis, J.Rose, Z.G.Vranesic, 2007 BSP
4. Digital Systems Design with FPGA's and CPLDs – Ian Grout, 2009, Elsevier
5. DSP architectures by avathar singh & srinivasan

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M. TECH-DSCE-I SEMESTER

DIGITAL CONTROL SYSTEMS

(Elective II)

UNIT : SIGNAL CONVERSION AND PROCESSING

Introduction, Digital Signals and Coding, Data Conversion and Quantization, Sample and Hold Devices, Digital to Analog conversion, Analog to Digital conversion, Mathematical modeling of the sampling process, Sampling theorem, Mathmatical modeling of sampling by convolution integral, Flat Top approximation of the finite-pulse width sampling, Data reconstruction and filtering of sampled signals, Zero order hold first order hold and Polygonal hold and slewer hold.

Review of Z- Transform and Applications

Review of Z- Transform, Applications of Z-Transform, Signals between sampling instants-Submultiple sampling method & Delayed Z- Transform and the modified Z- Transform.

UNIT II : TRANSFER FUNCTIONS, BLOCK DIAGRAMS, AND SIGNAL FLOW GRAPHS

Introduction, Pulse Transfer Function and Z – Transfer function, Relation between G(s) and G(z), Closed loop systems, Sampled Signal Flow Graph, Modified Z – Transfer function, multirate Discrete Data Systems, (Slow Fast, Fast-Slow, Multirate Systems with all Digital systems, closed loop multi sampled

Controllability, Observability and Stability

Introduction, Controllability of Linear Time invariant Discrete Data systems, Observability and Transfer functions, Stability of Linear Digital Control systems, Stability tests of Discrete Data systems (Bilinear Transformation method – Extension of the RH criterion, Jurys stability test)

UNIT III : TIME DOMAIN AND Z – DOMAIN ANALYSIS Introduction, Prototype Second Order system, Comparison of Time Responses of Continuous Data and Discrete Data systems, Steady State Error analysis of Digital Control systems, Correlation between time response and root locations in S – plane and Z – plane, Dominant Characteristic Equation, Root loci of Digital Control systems, Effects of adding poles and zeroes to Open loop transfer function

Frequency Domain Analysis

Introduction, Polar plot of GH (z), Nyquist Stability criterion Bode plot, Gain Margin and Phase Margin, Bandwidth considerations, and Sensitivity analysis

UNIT IV : DESIGN OF DISCRETE DATA CONTROL SYSTEMS

Introduction, Cascade Compensation by continuous data Controllers, Design of Continuous data Continuous data Controllers, Design of Digital Control systems with Digital controllers and Bilinear transformation

UNIT: STATE VARIABLE TECHNIQUE:

State Equation of Discrete Data systems with Sample and Hold Devices, State equation of Digital Systems with All-Digital Elements, The State Transtions(the recursive method and the z-transform method), Relations between State Equation and Transfer Functions, Characteristic Equation, Eigen Vectors, Methods of Com putting the Transition Matrix (The cayley Hamilton Theorem. The Z-Transform Method), State Diagrams of Digital Systems, Decomposition of Discrete-Data Transfer Functions.

Text Books:

1. Digital Control Systems –Kuo, Second Edition, Oxford.

References:

1. Discrete – time Control Systems-Kstsuhiko Ogata, Second Edition, PHI.
2. Digital Control and State variable Methods (Conventional and intelligent Control Systems) . M. Gopal . Third Edition, TMH,

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M. TECH-DSCE-I SEMESTER

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INTERNET WORKING
(Elective IV)

UNIT – I:

Internetworking concepts: Principles of Internetworking, Connectionless Internetworking, Application level Interconnections, Network level INTERCONNECTION, Properties of the internet, Internet Architecture, Wired LANS, Wireless LANs, Point-to-Point WANs, Switched WANs, Connecting Devices, TCP/IP Protocol Suite.

IP Address: Classful Addressing: Introduction, Classful Addressing, Other issues, Sub-netting and Super netting.

IP Address: Classless Addressing – Variable length Blocks, Sub-netting, Address Allocation Delivery Forwarding and Routing of IP Packets: Delivery, Forwarding, Routing, Structure of Router

ARP and RARP: ARP, ARP Package, RARP

Unit – II:

Internet Protocol (IP): Datagram, Fragmentation, Option, Checksum, IP V.6.

Transmission Control Protocol (TCP): TCP Services, TCP Features, Segment, A TCP connection State Transition Diagram, Flow Control Error Control Congestion Control, TCP Times.

Stream Control Transmission Protocol (SCTP): SCTP Services, SCTP Features, Packet Format, Flow Control, Error Control, Congestion Control.

Mobile IP: Addressing, Agents, Three Phases, Inefficiency in Mobile IP

Classical TCP Improvements: Indirect TCP, Snooping TCP, Mobile TCP, Fast Retransmit/Fast Recovery, Transmission/Time Out Freezing, Selective Retransmission, Transaction Oriented TCP.

Unit – III:

Unicast Routing Protocols (RIP, OSPF, and BGP): Intra and Inter-domain Routing, Distance Vector Routing, RIP, Link State Routing, OSPF, Path Vector Routing, BGP.

Multicasting and Multicast Routing Protocols: Unicast – Multicast – Broadcast, Multicast Applications, Multicast Routing, Multicast Link State Routing, MOSPF Multicast Distance Vector DVMRP.

Unit – IV:

Domain Name System (DNS): Name Space, Domain Name Space, Distribution of Name Space and DNS in the internet.

Remote Login TELNET:- Concept, Network Virtual Terminal (NVT). **File Transfer FTP and TFTP:** File Transfer Protocol (FTP) **Electronic Mail:** SMTP and POP.

Network Management SNMP: Concept, Management Components. World Wide Web- HTTP Architecture.

Unit-V

Multimedia Digitizing Audio and Video, Network security, security in the internet firewalls, Audio and Video compression, streaming Stored Audio/Video, Streaming Live ?Audio/Video, Real-Time Interactive Audio/Video, RTP, RTCP, Voice Over IP Network Security, Security in the internet, Firewells.

Text Books:

TCP/IP Protocol Suite-Behrouz A.Forouzan, Third Edition, TMH
Internetworking with TCP/IP Corner 3rd edition PHI

Reference:

High Performance TCP/IP Networking . Mahbub Hassan, Raj Jain, PHI, 2005
Date Communications & Networking-B.A. Forouzan – 2nd Edition – TNH

High Speed Networks and Internets – William Stallings, Pearson Education, 2002, Data and Computer Communications, William Stallings, 7th Edition, P.

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M. TECH-DSCE-I SEMESTER

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SIMULATION LAB (VHDL/VERILOG)

(A Minimum 11 Experiments have to be Performed)

1. Simulation and Verification of Logic Gates
2. Design and Simulation of adder, Serial Binary Adder Multi Precession Adder, Carry Look Ahead Adder.
3. Simulation and verification of Decoder, MUXs, Encoder using all Modelling Styles.
4. Modelling of Flip-Flops with Synchronous and Asynchronous reset
5. Design and simulation of Counters- Ring Counter, Johnson Counter, Up-Down Counter Ripple Counter.
6. Design of a N-bit Register of Serial- in Serial-out, Serial in parallel out, Parallel in Serial out and Parallel in Parellel Out.
7. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines)
8. 4- Bit Multiplier, Divider.
9. ALU to Perform – ADD SUB AND-OR 1'S AND 2'S compliment, Multiplication Division.
10 Verification of the Functionality of the Circuit using function Simulators.
11 Timing Simulator for Critical Path time Calculation
12 Sytjesis of Digital Sircuit
13 Place and Router Techniques for FPGA's like Xilinx, Altera Cypress, etc, Implementation or Design using FPGA and CPLD Devices.

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M. TECH-DSCE-II SEMESTER			
ADVANCED COMPUTER ARCHITECTURE	**-**	**- / 3 /-**	**3**

Unit I

Concept of instruction format, and instruction set of a computer, types of operands and operations addressing modes processor organization register organization and stack organization instruction cycle basic datival of Pentium processor and power pc processor

RISC &CISC instructions set

Unit II

Memory devices, semiconductors and ferrite core memory main memory, Cache memory associative memory organization, concept of virtual memory organization and mapping, partitioning demand paging and, segmentation Magnetic disc organization introduction to Magnetic tape and CDROM

Unit III

IO devices programmed IO , interrupt driver IO , DMA IO modules IO addressing IO channels IO processors DOTMATRIX printers, LASER printer, INKJET printer. Advanced concepts, horizontal and vertical instruction format micro programming Micro instruction sequence and control instruction pipeline parallel processing ,problems in parrllel processing data hazards and control hazards

Unit IV

ILP software approach ,compiler techniques ,static branch protection VLIW approach-H W support for more ILP at compile time – H. W Vs SW solutions

Multiprocessor thread level and parallelism –symmetric shared memory architectures distributed shared memory synchronization multithreading

Unit V

Storage systems types – buses RAID errors and failures bench markings a storage device designing's input and output systems interconnection networks clusters interconnection network media practical issues in interconnecting networks examples clusters designing a clusters

Text books :

1. Computer organization and architecture wiliam stallings PHI india 1998
2. Computer organization carl Hamachar,zvonko varanisik
3. Computer architecture & organization John P. hayes

Reference Books

1. Computer architecture a quantitative approach 3rd edition john L. Hannessy& David A. Patteson

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M. TECH-DSCE-II SEMESTER

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LOW POWER VLSI DESIGN

UNIT – I

Low Power Design – An over view: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS Process: Bi CMOS processes, Integration and Isolation considerations, integrated Analog/Digital CMOS Process.

UNIT – II

Low Voltage/Low Power CMOS/BiCMOS Processes: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/BiCMOS processes.

UNIT III

Device Behavior and Modeling: Advanced MOSFET models, limitations of MOSFET models, bipolar models.

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid-mode environment.

UNIT IV

CMOS and Bi-CMOS Logic Gates: Conventional CMOS and BiCMOS logic gates, Performance evaluation

Low Voltage Low Power Logic Circuits: Comparison of advanced BiCOMS Digital circuits, ESD-free Bi CMOS, Digital circuit operation and comparative Evaluation.

UNIT V

Low Power Latches and Flip Flops: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

Text Books:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors) – Pearson Education Asia 1st Indian reprint, 2002

References:

1. Digital integrated circuits – J.M. Rabaey, PH. N.J.1996
2. CMOS Digital Integrated Circuits Analysis & Design – Sung-Mokang, Yosuf Lleblebici 3rd ed., 2003, TMH 2003.
3. VLSI DSP Systems – K.K. Parhi, 1999, John Wiley & Sons.
4. IEEE Trans Electron Devices, IEEE J. Solid State Circuits, and other National and International Conferences and Symposia.

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M. TECH-DSCE-II SEMESTER

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DESIGN OF FAULT TOLERANT SYSTEMS

UNIT – I

FAULT TOLERANT DESIGN

Basic Concepts: Reliability Concepts, Failure & Faults, Reliability and Failure rate, Relation between Reliability and Meantime between failure, Maintainability and Availability, Reliability of series, parallel and Parallel – Series combinational circuits.

Fault Tolerant Design: Basic Concepts – Static, dynamic, hybrid Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), 5 MR Re-Configuration techniques, Use of error correcting code. Time redundancy and software redundancy

UNIT – II

SELF CHECKING CIRCUITS & FAIL SAFE DESIGN

Self Checking circuits: Basic concepts of self checking circuits, Design of Totally self checking checker, checkers using m out of n codes, Berger code, Low Cost residue code.

Fail Safe Design: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA Design

UNIT – III

ATPG FUNDAMENTALS & DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUIT

Introduction to ATPG, ATPG Process – Testability and Fault analysis methods – Fault masking – Transition delay fault ATPG, Path delay, fault ATPG

Design for Testability for Combinational Circuits : Basic concepts of Testability, Controllability and Observability, The Reed Muller's expansion technique, OR-AND-OR Design, Use of control and Syndrome Testable Designs

UNIT – IV

SCAN ARCHITECTURES & TECHNIQUES

Introduction to Scan Based testing, Functional testing, The Scan effective Circuit, The MUX-D Stule Scan flip-flops, The Scan shift register, scan cell operation

Scan test sequencing, scan testing timing, partial scan, multiple scan chains, scan based design rules (LSSD) At-speed scan testing and Architecture, multiple clock and scan domain operation, critical paths for At speed scan test.

UNIT – V

BUILT IN SELF TEST (BIST)

BIST concepts, Tests Pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture, Memory Test architecture.

Text Books:

1. Fault Tolerant & Fault Testable Hardware Design – Parag K. Lala, 1984, PHI
2. Design for Test for Digital IC's and Embedded Core Systems – Alfred L. Crouch 2008, Pearson Education.

Reference Books:

1. Digital Systems Testing and testable Design – Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, Jaico Books

2. Essentials of Electronic Testing – Bushnell & Vishwani D.Agarwal, Springers.

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M. TECH-DSCE-II SEMESTER

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EMBEDDED SYSTEM DESIGN VIA RTOS

UNIT I :- Introduction to Embedded systems categories, overview of Embedded system Architecture, Specifications of Embedded system, Recent Trends in Embedded systems.
Architecture of Embedded systems:- Hardware Architecture, Software Architecture, Application software, Communication software, Development Testing Tools. Embedded system Development, Development process. Requirements, Design, Implementation, Integrating and Testing, Packing, Configuration management.
Hardware Platforms:- Types of Hardware platforms, AVR microcontroller Development Board. Software Development:- Quality Programming ,memory Allocation, Self Documenting code, modular software development layered software systems Device Drivers, Object oriented Interfacing Threads, Recursion, Debugging Strategies
UNIT II :- Embedded/Real-Time Operating System Concepts:- Architecture of the Kernel, Task and Task Scheduler-clock driven, weighted round robin, priority driven. Interrupt Service Routines, Semaphores, Mutex, Mailboxes, message Queues, Event Registers, Pipes, Signals, Timers, Memory management Priority Inversion Problem.Inter-process communication and synchronization of processes
UNIT III :-Interfacing: Communication Interface RS232, USB, Infrared, IEEE 802.11, Ethernet, Bluetooth . Parallel port interfaces input switches and keyboards, High speed I/O interfacing:- Need for speed, High speed I/O applications, Approaches to High speed Interfaces.

Embedded system Applications using INTEL ARM platform ;Architecture of Prayog, Applications, RFID systems**..** Design Technology: Introduction, Automation synthesis, Logical Behavioural, system synthesis, Hardware and software co-design, Verification, Emulators, Reuse IP cores, Design process models.

UNIT-IV:

Typical real time applications, hard vs soft real-time systems. overview of unix. A reference model of real time systems: processors and resources, temporal parameters of real time work load, periodic task model precedence constraints and data dependency, functional parameters, resources parameters of jobs and parameters of resources.

UNIT V:

Operating systems services, i/o subsystems, rt & embedded systems os, interrupt routine in rtos environment. Introduction to Vx works , features of VX works. case study of an embedded system for a smart card. case study of sending application layer byte streams on a tcp/ip network.

TEXT BOOKS:

Embedded Real Time systems concepts Design and Programming by Dr.K.V.K.K.Prasad ;
DreamTech publications
Embedded Micro computer Systems (Real Time Interfacing) by Jonathan W.Valvano Thomson publications
Embedded system Design (2nd Edition) Steve Heath Elsever publications
Embedded system Design (A unified Hardware/Software Introduction) (Frank Vahid /Tony Givargis) Wiley publications.

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M. TECH-DSCE-II SEMESTER
SYSTEM ON CHIP ARCHITECTURE
(Elective III)

UNIT – I:
Introduction to Processor Design: Abstraction in Hardware Design, MUO a simple processor, Processor design trade off, Design for low power consumption
ARM Processor as System-on-Chip: Acom RISC Machine – Architecture inheritance – ARM programming model – ARM development tools – 3 and 5 stage pipeline ARM organization – ARM instruction execution and implementation – ARM Co-processor interface
UNIT – II:
ARM Assembly Language Programming: ARM instruction types – date transfer, date processing and control flow instructions – ARM instruction set – Co-processor instructions.
Architectural Support for High Level Language: Data types – abstraction in Software design – Expressions – Loops – Functions and Procedures – Conditional Statements – Use of Memory.
UNIT – III:
Memory Hierarchy: Memory size and speed – On-chip memory – Caches – Cache design – an example – memory management
UNIT – IV:
Architectural Support for System Development: Advanced Microcontroller bus architecture – ARM memory interface – ARM reference peripheral specification – Hardware System prototyping tools – Armulator – Debug architecture

UNIT – V
Architectural Support for Operating System: An introduction to Operating Systems – ARM system control coprocessor – CP 15 protection unit registers – ARM protection unit – CP15 MMU registers – ARM MMU Architecture – Synchronization – Context Switching input and output

Text Books:
1. ARM system on Chip Architecture – Steve Furber – 2nd ed. 2000, Addison Wesley Professional
2. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st ed. 2004, Springer

References:
1. Co-Verification of Hardware and Software for ARM system on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM
2. System on Chip Verification – Methodologies and Techniques – Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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M. TECH-DSCE-II SEMESTER

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NETWORK SECURITY AND CRYPTOGRAPHY
(Elective III)

UNIT-I:
Attacks, Services and Mechanisms, Security attacks, Security Services. A model for internetwork security, Classical Techniques, Conventional Encryptional model, Steganography, Classical Encryption Techniques.
Modern Techniques: Simplified DES, Block Cipher Principles, Data Encryption Standard, Strength of DES, Differential and Linear Cryptanalysis Block Cipher Design Principles and Modes of operations.
UNIT – II
Algorithms: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.
Conventional Encryption Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.
Number theory Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.
Public Key Cruptography: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography
UNIT-III
Message authentication and Hash functions:
Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs..
Hash and Mac Algorithms:MD File, Message digest Alborithm, Secure Hash Algorithm, RIPEMD-160, HMAC **Digital Singnatures and Authentication protocols**
Digital signatures, Authentication Protocols, Digital signature standards
UNIT-IV
Authentication Applications Kerbores, X.509 directory Authentication service.
Electronic Mail Security Pretty Good Privary S/MIME/
UNIT-V
IP Security Overview, Architecture Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
Web Security: Web Security requirements, Secure sockets layer and Transport layer security, Secure Electronic Transaction.
Intruders, Viruses and Worms : Intruders, Viruses and Related threats
Fire Walls : Fire Wall Design Principles, Trusted Systems.
Text Books:

1. Cryptography and Network Security Principles and Practice – William Stallings, 2000, PE

REFERENCE BOOKS:

1. Principles of Network and Systems Administration, Mark Burgess, John Wiel.

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M. TECH-DSCE-II SEMESTER

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ROBOTICS

(Elective III)

UNIT-I: INTRODUCTION & BASIC DEFINITIONS

Introduction, Control Programs for Robots, Industry Applications of Robots, Pick and Place, Gantry and Arm type Robots in typical set-ups like Automobile Industry

Coordinate Systems : Cartesian, Cylindrical, Polar, and Revolute Systems: Robot Positioning: Robot Arms; Axes, their ranges, offset and In-line Wrist; Roll, pitch and Yaw, their meaning in Robotics

UNIT-II : MECHANICAL ASPECTS

Kinematics, Inverse Kinematics, Motion Planning and Mobile Mechanisms

UNIT-III : SENSORS AND APPLICATIONS

Range and use of Sensors, Microswitches, Resistance Transducers, Piezo-electric, Infrared and Lasers

Applications of Sensors : Reed Switches, Ultrasonic, Barcode Readers and RFID

UNIT-IV : ROBOT SYSTEMS

Hydraulic and Electrical Systems including pumps, valves, solenoids, cylinders, stepper motors, Encoders and AC Motors

UNIT-V : PROGRAMMING OF ROBOTS

Programming of Robots such as Lego Robots, Programming environment, Example Applications, Safety considerations.

Text Books:

1. Introduction to Robotics – P.J.Mckerrow, ISBN : 0201182408
2. Introduction to Robotics – S.Nikv, 2001, Prentice Hall,
3. Mechatronics and Robotics : Design & Applications– A.Mutanbara, 1999, CRC Press

Reference Books:

1. Robotics – K.S.Fu, R.C.Gonzalez and C.S.G. Lee, 2008, TMH.

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M. TECH-DSCE-II SEMESTER

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CMOS ANALOG MIXED SIGNAL DESIGN

(Elective IV)

CMOS ANALOG CIRCUITS:

Current Sources & Sinks: The cascade connection, sensitivity and temperature analysis, transient response, layout of simple Current Mirror, matching in MOSFET mirrors, other Current Sources/Sinks. Voltage dividers, current source self-biasing, band gap voltage references, Beta-Multiplier Referenced Self-biasing.

UNIT-II:

Amplifiers: Gate Drain connected loads, Current source loads, Noise and distortion, Class AB Amplifier.

Feedback Amplifiers: Feedback Equation, properties of negative feedback and amplifier design, feedback topologies, amplifiers employing the four types of feedback, Stability.

UNIT-III:

Differential Amplifiers: The source coupled pair, the source cross-coupled pair, cascade loads, Wide-Swing Differential Amplifiers,

Operational Amplifiers: Basic CMOS Op-Amp Design, Operational Trans conductance Amplifiers, Differential Output OP-Amp

MIXED SIGNAL CIRCUITS:

UNIT-IV:

Non-Linear & Dynamic Analog Circuits: Basic CMOS Comparator Design, Adaptive Biasing, Analog Multipliers, MOSFET Switch, Switched Capacitor circuits: Switched Capacitor Integrator, dynamic circuits.

UNIT – V:

Data Converter Architectures: Date Converter Fundamentals, DAC & ADC specifications, Mixed Signal Layout issues, DAC architectures, ADC architectures.

Text Books:

1. CMOS Circuit Design, Layout and Simulation – Baker, Li, Bouyce, 1st ed., TMH

Reference Books:

1. Analog Integrated Circuit Design – David A.Johns, Ken Martin, 1997, John-Wiley & Sons
2. Design of Analog CMOS Circuits – B.Razavi, MGH, 2003, TMH
3. Analog MOS ICs for Signal Processing- R.Gregorian, Gabor C.Temes, John Wiley & Sons

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M. TECH-DSCE-II SEMESTER

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DIGITAL SIGNAL PROCESSORS AND ARCHITECTURES

(Elective IV)

UNIT 1:

INTRODUCTION TO DIGITAL SIGNAL PROCESSING

Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS

Number formats for signals and coefficients in DSP Systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors D/A Conversion Errors, Compensating filter.

UNIT II

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES

Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT III:

EXECUTION CONTROL AND PIPELINING

Hardware looping, interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Date Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Procesors.

UNIT IV:

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS

The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

IMPLEMENTATION OF FFT ALGORITHMS

An FFT Algorithm for DFT Computation, a Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT Implementation on the TMS320C54XX, Computer computation of the signal spectrum.

UNIT V:

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES

Memory Space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O Interrupts and I/O, Direct memory access (DMA)

A Mulchannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit. CODEC programming, A CODEC – DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S.Sriniasan, Thomson Publications 2004
2. DSP Processor Funamentals, Architectures & Features – Lapsley et al. 2000, S.Chand & Company

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M.Bhaskar, 2002, TMH

2. Digital Signal Processing – Johatham Stein, 2005, John Wiley.

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ARTIFICIAL INTELLIGENCE

Elective IV

UNIT – I:

ARTIFICIAL INTELLIGENCE

Definition, study of A1 techniques problem & problem spaces, Heuristis search problem chavacteristics.

SEARCHING METHODS

Breadth first search, depth first search, generate & test Hill Climbing, best-first search, problems reduction, constraint satisfaction, means-end analysis

UNIT-II:

BASIC PROBLEM SOLVING METHODS

Forward versus backward reasoning, problem trees, graphs, matching, game playing, minimax algorithms, alphabeta heuristics.

UNIT-III

Knowledge representation using predicate logic:

Prepositional logic, representing simple facts in logic resolution unification question answering, introduction to prolog and LISP.

Structured knowledge representations

Declarative representation semantic nets, frames scripts procedural representation.

UNIT-IV

Natural language understanding

Introduction semantics analysis augmented transition networks semantic analysis semantic grammars

UNIT – V

Computer vision

Perception processing representation and recognitions of scents, understanding as constraints satisfaction determining to constraints, Waltz algorithms.

Expert Systems

Representing and using domain knowledge, expert system shells, explanation knowledge acquisition, case studies.

Text Books:

1. Artificial Intelligence, Elaine. Rich
2. Artificial Intelligence, 2nd Edition, E.Rich and K.Knight (TMH)
3. Principles of Artificial Intelligence by Nilsson
4. D.A.WATERMAN Expert systems.

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EMBEDDED SYSTEMS DESIGN LAB
(A Minimum of 12 Experiments Have To Be Performed)

1) Serial data transmission using 8051 microcontroller in different modes.
2) Lookup tables for 8051
3) Timing subroutines for 8051-realtime times and applications
4) Key board interface to 8051
5) ADC DAC interface to 8051
6) LCD interface to 8051
7) Study of realtime operating systems
8) Development of device drivers for RT Linux
9) Software development for DSP applications
10) Serial communications drivers for arm processors
11) Case studies any two
12) Design of RT OS kernel
13) Cross compiler/assembler
14) Vx works